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WHAT IS CLAIMED IS:

1. A buffer/driver circuit having one or more inputs and an output for driving a load comprising:

a first logic circuit path having one or more buffer inputs and a buffer output; and

a second logic circuit path receiving the one or more buffer inputs and generating a first logic output coupled to the buffer output, wherein the first logic output enhances a current drive capability of a first logic state of the buffer output in response to a first logic combination of the one or more buffer inputs and a first logic state of a first control signal, and a first power supply voltage is coupled to the second logic path by a first electronic switch in response to the first logic state of the first control signal and decoupled from the second logic path in response to a second logic state of the first control signal.

2. The buffer/driver circuit of claim 1 further comprising a third logic circuit path receiving the one or more buffer inputs and generating a second logic output coupled to the buffer output, wherein the second logic output enhances a current drive capability of a second logic state of the buffer output in response to a second logic combination of the one or more buffer inputs and a second logic state of a second control signal and a second power supply voltage is coupled to the third logic path by a second electronic switch in response to the second logic state of the second control signal and decoupled from the third logic path in response to the first logic state of the second control signal.

3. The buffer/driver circuit of claim 1, wherein the first logic path comprises:

a first logic circuit receiving the one or more buffer inputs and generating an intermediate logic output as a logic combination of the one or buffer inputs; and

an inverter having an input coupled to the intermediate logic output and an output forming the first logic output.

4. The buffer/driver circuit of claim 3, wherein the second logic circuit path comprises:

a first power-gated logic circuit having a positive power supply node coupled to the second power supply voltage, a negative power supply node, one or more logic inputs coupled to the buffer inputs, and an intermediate logic output generating the first logic state in response to a logic combination of logic states of the one or more logic inputs and generating the second logic state at the intermediate logic output in response to the first logic combination of the logic states of the one or more buffer inputs and the first logic state of the first control signal, wherein the first electronic switch has a first node coupled to the first power supply voltage, a second node coupled to the negative power supply node, and a control input coupled to the first control signal; and

a power PFET having a gate coupled to the intermediate logic output of the first power-gated logic circuit, a source coupled to a second power supply voltage and a drain forming the first logic output.

5. The buffer/driver circuit of claim 2, wherein the third logic path comprises:

a second power-gated logic circuit having a negative power supply node coupled to the first power supply voltage, a positive power supply node, one or more logic inputs coupled to the buffer inputs, and an intermediate logic output generating the second logic state in response to the logic combination of logic states of the one or more logic inputs and generating the first logic state at the intermediate logic output in response to the first logic combination of the logic states of the one or more buffer inputs and the second logic state of the second control signal, wherein the second electronic switch has a first node coupled to the second power supply voltage, a

second node coupled to the negative power supply node, and a control input coupled to the second control signal; and

a power NFET having a gate coupled to the intermediate logic output of the second power-gated logic circuit, a source coupled to the first power supply voltage and a drain forming the second logic output.

6. The buffer/driver circuit of claim 4, wherein the first electronic switch comprises an NFET having a source coupled to the first node, a gate coupled to the first control signal and a drain coupled to the second node, wherein the NFET couples the first power supply voltage to the first power-gated logic circuit in response to the first logic state of the first control signal.

7. The buffer/driver circuit of claim 5, wherein the second electronic switch comprises a PFET having a source coupled to the first node, a gate coupled to the second control signal, and a drain coupled to the second node, wherein the PFET couples the second power supply voltage to the second power-gated logic circuit in response to the second logic state of the second control signal.

8. A buffer/driver circuit having one or more buffer inputs and a buffer output for driving a load comprising:

a first logic circuit path having one or more inputs coupled to the buffer inputs, a first output, a first buffer output, and a second buffer output;

a second logic circuit path receiving one or more buffer inputs and generating a first logic output coupled to the first buffer output, wherein the first logic output enhances a current drive capability of a first logic state of the first buffer output in response to a first logic combination of the one or more buffer inputs and a first logic state of a first control signal, and a first power supply voltage is coupled to the second logic circuit path by a first electronic switch in response to the first logic state of the first control signal and decoupled from the second logic circuit path in response to a second logic state of the first control signal; and

a third logic circuit path receiving the first output and generating a second logic output coupled to the second buffer output, wherein the second logic output enhances a current drive capability of a second logic state of the second buffer output in response to the first logic combination of the one or more buffer inputs and a second logic state of a second control signal, and a second power supply voltage is coupled to the third logic circuit path by a second electronic switch in response to the second logic state of the second control signal and decoupled from the third logic circuit path in response to the first logic state of the second control signal.

9. A data processing system comprising:

a central processing unit (CPU);

a random access memory (RAM);

an input output (I/O) interface unit; and

a bus for coupling the CPU, RAM and I/O interface unit, wherein the CPU has a buffer/driver circuit having a first logic circuit path with one or more buffer inputs and a buffer output, a second logic circuit path receiving the one or more buffer inputs and generating a first logic output coupled to the buffer output, wherein the first logic output enhances a current drive capability of a first logic state of the buffer output in response to a first logic combination of the one or more buffer inputs and a first logic state of a first control signal, and a first power supply voltage is coupled to the second logic path by a first electronic switch in response to the first logic state of the first control signal and decoupled from the second logic path in response to a second logic state of the first control signal.

10. The data processing system of claim 9 further comprising a third logic circuit path receiving the one or more buffer inputs and generating a second logic output coupled to the buffer output, wherein the second logic output enhances a current drive capability of a second logic state of the buffer output in response to a second logic combination of the one or more buffer inputs and a second logic state of a second control signal and a second power supply voltage is coupled to the third logic path by a second electronic switch in response to the second logic state of the second control signal and decoupled from the third logic path in response to the first logic state of the second control signal.

11. The data processing system of claim 9, wherein the first logic path comprises:

a first logic circuit receiving the one or more buffer inputs and generating an intermediate logic output as a logic combination of the one or buffer inputs; and

an inverter having an input coupled to the intermediate logic output and an output forming the first logic output.

12. The data processing system of claim 11, wherein the second logic circuit path comprises:

a first power-gated logic circuit having a positive power supply node coupled to the second power supply voltage, a negative power supply node, one or more logic inputs coupled to the buffer inputs, and an intermediate logic output generating the first logic state in response to a logic combination of logic states of the one or more logic inputs and generating the second logic state at the intermediate logic output in response to the first logic combination of the logic states of the one or more buffer inputs and the first logic state of the first control signal, wherein the first electronic switch has a first node coupled to the first power supply voltage, a second node coupled to the negative power supply node, and a control input coupled to the first control signal; and

a power PFET having a gate coupled to the intermediate logic output of the first power-gated logic circuit, a source coupled to a second power supply voltage and a drain forming the first logic output.

13. The data processing system of claim 10, wherein the third logic path comprises:

a second power-gated logic circuit having a negative power supply node coupled to the first power supply voltage, a positive power supply node, one or more logic inputs coupled to the buffer inputs, and an intermediate logic output generating

the second logic state in response to the logic combination of logic states of the one or more logic inputs and generating the first logic state at the intermediate logic output in response to the first logic combination of the logic states of the one or more buffer inputs and the second logic state of the second control signal, wherein the second electronic switch has a first node coupled to the second power supply voltage, a second node coupled to the negative power supply node, and a control input coupled to the second control signal; and

a power NFET having a gate coupled to the intermediate logic output of the second power-gated logic circuit, a source coupled to the first power supply voltage and a drain forming the second logic output.

14. The data processing system of claim 12, wherein the first electronic switch comprises an NFET having a source coupled to the first node, a gate coupled to the first control signal and a drain coupled to the second node, wherein the NFET couples the first power supply voltage to the first power-gated logic circuit in response to the first logic state of the first control signal.

15. The data processing system of claim 13, wherein the second electronic switch comprises a PFET having a source coupled to the first node, a gate coupled to the second control signal, and a drain coupled to the second node, wherein the PFET couples the second power supply voltage to the second power-gated logic circuit in response to the second logic state of the second control signal.

16. A data processing system comprising:

a central processing unit (CPU);

a random access memory (RAM);

an input output (I/O) interface unit;

a bus for coupling the CPU, RAM and I/O interface unit, wherein the CPU has a buffer/driver circuit having a first logic circuit path having one or more inputs coupled to the buffer inputs, a first output, a first buffer output, and a second buffer output, a second logic circuit path receiving one or more buffer inputs and generating a first logic output coupled to the first buffer output, wherein the first logic output enhances a current drive capability of a first logic state of the first buffer output in response to a first logic combination of the one or more buffer inputs and a first logic state of a first control signal, and a first power supply voltage is coupled to the second logic circuit path by a first electronic switch in response to the first logic state of the first control signal and decoupled from the second logic circuit path in response to a second logic state of the first control signal, and a third logic circuit path receiving the first output and generating a second logic output coupled to the second buffer output, wherein the second logic output enhances a current drive capability of a second logic state of the second buffer output in response to the first logic combination of the one or more buffer inputs and a second logic state of a second control signal, and a second power supply voltage is coupled to the third logic circuit path by a second electronic switch in response to the second logic state of the second control signal and decoupled from the third logic circuit path in response to the first logic state of the second control signal.